Design Techniques for EMC
Part 5 — Printed Circuit Board (PCB) Design and Layout

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This is the **fifth** in a series of six articles on basic good-practice electromagnetic compatibility (EMC) techniques in electronic design, to be published during 2006-7. It is intended for designers of electronic modules, products and equipment, but to avoid having to write modules/products/equipment throughout – everything that is sold as the result of a design process will be called a 'product' here.

This series is an update of the series first published in the UK EMC Journal in 1999 [1], and includes basic good EMC practices relevant for electronic, printed-circuit-board (PCB) and mechanical designers in all applications areas (household, commercial, entertainment, industrial, medical and healthcare, automotive, railway, marine, aerospace, military, etc.). Safety risks caused by electromagnetic interference (EMI) are not covered here; see [2] for more on this issue.

These articles deal with the practical issues of what EMC techniques should generally be used and how they should generally be applied. Why they are needed or why they work is not covered (or, at least, not covered in any theoretical depth) – but they are well understood academically and well proven over decades of practice. A good understanding of the basics of EMC is a great benefit in helping to prevent under- or over-engineering, but goes beyond the scope of these articles.

The techniques covered in these six articles will be:
1) Circuit design (digital, analogue, switch-mode, communications), and choosing components
2) Cables and connectors
3) Filtering and suppressing transients
4) Shielding (screening)
5) PCB layout (including transmission lines)
6) ESD, surge, electromechanical devices, power factor correction, voltage fluctuations, supply dips and dropouts

Many textbooks and articles have been written about all of the above topics, so this magazine article format can do no more than introduce the various issues and point to the most important of the basic good-practice EMC design techniques. References are provided for further study and more in-depth EMC design techniques.

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5.5 Power supply decoupling

5.5.1 General decoupling design rules

Power rail decoupling aims to keep the noisy RF currents drawn by semiconductors from exciting the product's power distribution system (PDS) as an accidental antenna (see [7]) and increasing emissions. The technique uses decoupling capacitors ('decaps') to provide very low impedances at the frequencies of concern, local to the noisy semiconductors, which encourage the noisy currents to remain local and not spread through the PDS. Similarly, decoupling maintains a low impedance to improve immunity to a range of conducted transient and continuous EM phenomena that can exist on the power rail.

Every power pin on an IC (or other type of semiconductor) should have a nearby decap to its local RF Reference (its nearby 0V plane). Figure 5K shows the general guidelines for an IC with only a 0V plane; and for an IC that has an adjacent pair of 0V and power planes in its PCB stack-up (strongly recommended, see 5.5.3).

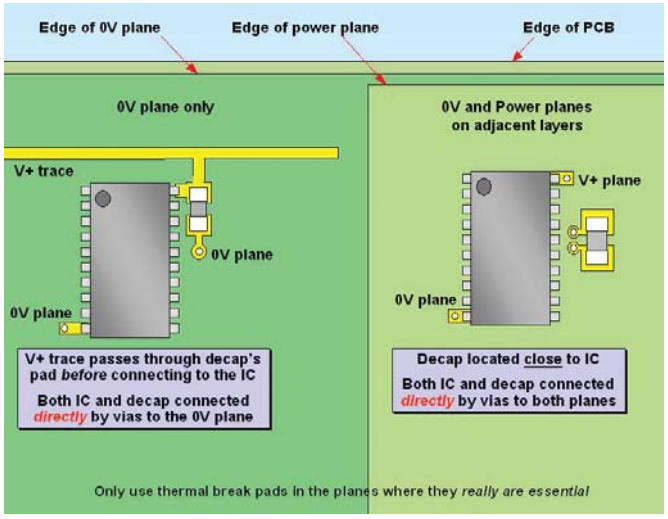

Figure 5K Examples of decoupling with planes

For the IC in Figure 5K that has only a 0V plane, the decap should be placed very close to the power pin, and the power trace should pass through the decap's pad before connecting to the IC. The 0V pins of the IC and of the decap itself should connect directly to the 0V plane using short wide traces. Where 0V *and* power planes are both available, the IC to be decoupled and the decap itself should connect directly to both planes using short wide traces.

Figure 5L shows an example of an IC with multiple sets of 0V and power pins, each of which should have at least one local decap.

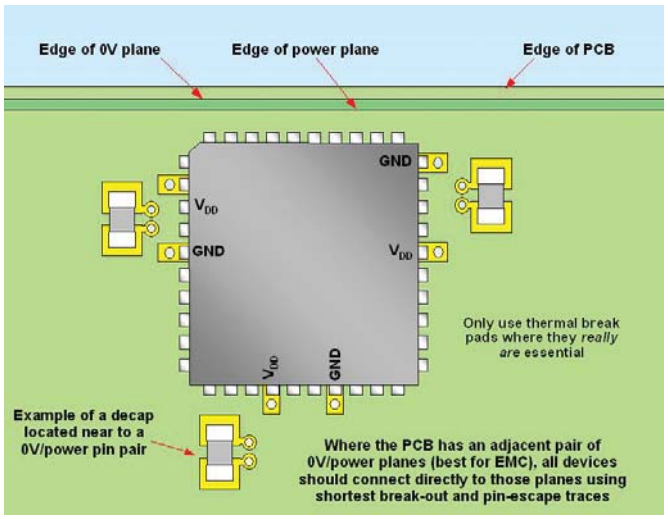

Figure 5L Another example of decoupling with planes

The RF impedance between two connections to a plane is orders of magnitude less than an equivalent length of trace, which is why we always use a plane instead of a trace where a plane is available. Some designers are in the habit of connecting IC pins to decaps using traces, and then connecting the decaps to the planes. Their intention is to 'keep the noise out of the planes' but, as described in 5.5.3, an adjacent pair of 0V and power planes is much better at decoupling noise frequencies above 300MHz than any discrete decaps possibly can – and modern digital ICs produce a great deal of power supply noise above 300MHz.

Also, the use of traces from IC to decap increases the total inductance of the decoupling, making the decaps much less effective at frequencies above 100MHz. So it is now best to use the layout techniques shown in Figure 5K and Figure 5L. The best discrete decaps are surface mounted multilayer ceramic capacitors (SMD MLCCs). Decaps with COG and NPO dielectrics generally have the best performance at the highest frequencies, but the lower cost X7R dielectrics are often better for EMC overall because their higher series resistance provides some useful damping for the resonances that plague PDSs.

The self-resonant frequency of a decap of capacitance C, is given by $1/\{2\pi\sqrt{(L_{tot}C)}\}$, where L_{tot} is the total inductance associated with the decap (the decap itself plus its associated pads, traces and via holes), and is almost always well below 100MHz. Above this frequency the decoupling of the noise on the power supply rails is provided by the inductive impedance of the decaps. So smaller decaps (e.g. 0402. 0201) with lower profiles, used with the better layouts from Figure 5G, are best for EMC because their L_{tot} is the lowest.

5.5.2 Decoupling with ferrites

PCBs carrying mostly analogue ICs, or where the number of digital components is not very large, are sometimes designed with soft ferrite ('RF suppresser') beads in series with the power rails of their ICs, and with a 0V plane but no power plane. The ferrite beads help to restrict an IC's power supply noise currents to its nearby decap, and so provide better EMC performance than the '0V plane only' example in Figure 5K.

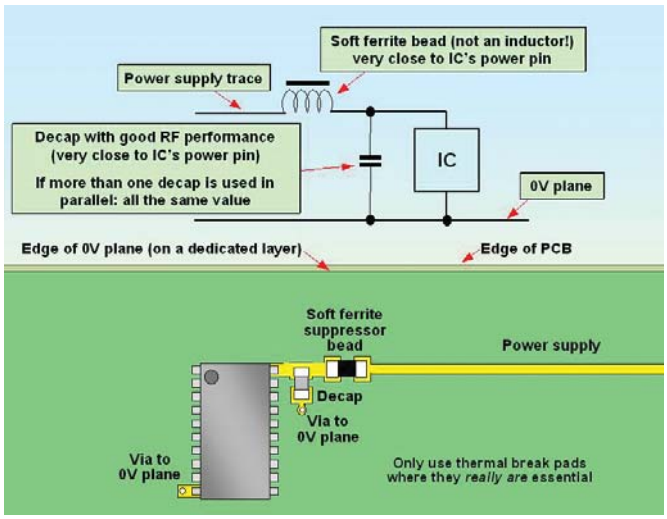

Figure 5M Example of decoupling with ferrites

For high-performance ICs, especially RF and analogue devices (e.g. ADSL drivers) the MLCCs used in this method may need to have better RF performance, which might mean using more costly types (e.g. the Murata ERB32 series). If more than one decap is used in parallel to achieve the desired total capacitance, they should all be the same value, to help avoid parallel resonances (which cause high impedances in the PDS).

Not all of the ICs on a board might need to use the ferrite beads, and some manufacturers spend longer in EMC test laboratories, replacing ferrites with zero-ohm links to reduce BOM costs by finding which ferrites are actually necessary.

5.5.3 Benefits of 0V/power plane pairs

As mentioned in 5.5.1, decoupling with discrete decaps relies on achieving a low inductance above 100MHz. But inductive impedance rises with frequency, so as frequencies exceed 300MHz decoupling schemes that rely on MLCCs (with/without ferrite beads, see 5.2.2) suffer higher impedances and hence emit more, and are also more susceptible to interference.

However, an adjacent pair of 0V and power planes in a PCB's layer stack provides an intrinsic, distributed capacitance that still behaves like a capacitor at well over 1GHz, due to its very low self-inductance. So these days it is generally recommended to include a 0V/power plane adjacent pair inside a PCB, to help achieve good decoupling above 300MHz.

For maximum benefit from a 0V/power plane pair, connect 0V and power pins and terminals of all devices and components directly to their respective planes, as shown in Figure 5K and Figure 5L. Any traces used to connect planes to the pins or pads of devices should be very short and wide to minimise their inductance (see Figure 5G).

Achieving low PDS impedance over the whole frequency range of concern these days requires a combination of decoupling techniques, as shown diagrammatically by Figure 5N.

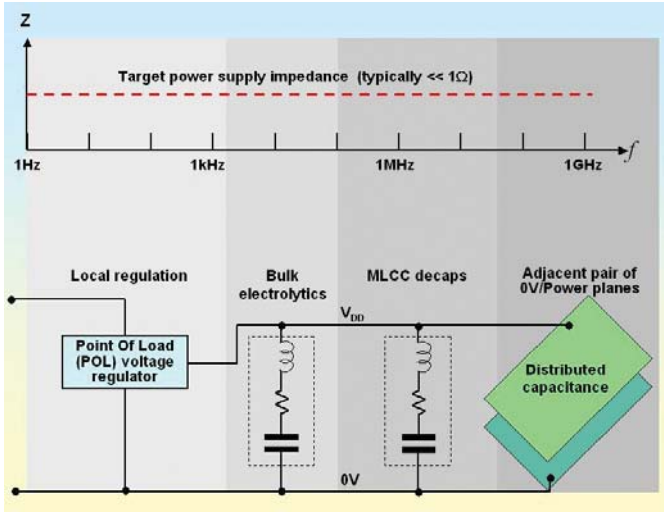

Figure 5N Achieving low PDS impedance to > 1GHz

5.5.4 Dealing with PDS resonances

When not using series ferrites in the PDS as in Figure 5M, decaps appear in parallel between the power and 0V – giving rise to parallel resonances, which cause high impedances that can cause EMC problems if any EM disturbances occur within their narrow ranges of frequencies. Also, 0V/power plane adjacent pairs can suffer cavity resonances due to their dimensions, which also cause high impedances.

Like all of the topics discussed in this article, [4] goes into a lot more detail on this issue, but it is enough for this basic guide to recommend the following approach to dealing with parallel resonances:

- If there are less than 10 decaps in total on the board – use same value (e.g. 10nF) for each
- If there are more than 10 decaps in total, use a range of values, e.g. 1, 2.2, 4.7, 10, 22nF, etc.
- Use the largest value capacitors available in the chosen package style (e.g. 0603).
- As well as placing decaps near to every power pin of every IC, also add more decaps all over the power plane, or along the power trace, so that they are no further apart from each other than $\lambda/10$ at f_{max} taking the board's dielectric constant into account ($15/f_{max}$ metres for FR4, where f_{max} is in MHz).
- Better still, use one of the several PDS simulators that have recently become available, to help decide on the above issues. If they are SI simulators rather than EMC, set 5 to 10 times lower limits for the PDS noise levels than are required just for the ICs to function correctly.
- Finally, verify the layout with 'proper' EMC tests.

The aim of these techniques is generally to ensure that whenever an IC's noisy power current cannot flow in its normal path, due to a parallel or cavity resonance at that frequency, there will be another path nearby that still has low impedance.

If resonances are still a problem, add series combinations of 4.7Ω resistors and 10nF MLCCs between the 0V and power to dampen down the peaks of the impedance resonances, at the locations on the board that provide the most benefit. The necessary experimentation can be begun with a spectrum analyser and close-field probe (parts 1 and 2 of [8]) on an ordinary development bench.

5.6 Matched transmission line techniques

5.6.1 When to use matched transmission lines

The digital industry guidance for good signal integrity (SI) – to achieve low-enough overshoots and ringing on the signals for reliable functionality – is to use a matched transmission line when the propagation time from the source to the load exceeds $t_r/2$, where t_r is the shortest rise-time carried by the trace (use fall-time instead, if it is less). Some digital designers recommend $t_r/3$ instead.

If working with a spectrum analyser rather than an oscilloscope, the $t_r/2$ 'rule' is equivalent to when the trace length exceeds $\lambda/7$ at f_{max}, taking the board's dielectric constant ε_r into account in the calculation of λ (approximately $24/f_{max}$ metres for an FR4 board, when f_{max} is in MHz).

The propagation time for a conductor in air is 3.3ps/mm, and for a conductor in a PCB dielectric it is $3.3\sqrt{\varepsilon_r}$ps/mm. The ε_r of FR4 is 4.2 (above 1MHz) so for an FR4 board we can assume a propagation time of about 6.6ps/mm (approximately 2ns per foot). So, for example, signals with 2ns risetimes would need to use transmission lines for trace lengths exceeding 150mm (about 6 inches), in an FR4 board.

But actual rise/fall-times are always much shorter than the data sheet specifications for an IC, and they get smaller each time the device undergoes a die shrink (which can be every couple of years, even for a mature part). ***And*** capacitive loading due to devices decreases the velocity of propagation and so increases the propagation time of a trace. So a 2ns (specified by the data sheet) IC driving a heavily loaded data bus might need to use matched transmission line techniques for traces longer than 40mm.

But the above guides are just for SI, not for EMC. To reduce cost-of-manufacture by improving EMC at PCB levels – reducing the need for costly and restrictive filtering and shielding – it will help to use matched transmission line techniques when traces are one-quarter of the lengths calculated above (preferably even less). In other words: use matched transmission lines when the source to load propagation time exceeds $t_r/8$, using the real rise-time value for t_r, not the data sheet value.

This 'rule' is equivalent to when the trace length exceeds $\lambda/28$ at f_{max}, taking the board's ε_r into account (approximately $6/f_{max}$ metres for an FR4 board, when f_{max} is in MHz. f_{max} in GHz gives the answer in mm).

Don't forget that capacitive loading by devices connected along a trace increase its propagation time (appropriate calculations are given in 5.6.2).

RF and microwave designers work with devices that must be connected to transmission lines with specified values of Z_0, for those devices to function correctly.

Many designers apply transmission line techniques to the signals that they already know need to use them. But for good EMC all traces should be analysed in terms of rise-times (or high-frequency content). It can happen that even traces to test points might need to be treated as transmission lines for EMC purposes. The analysis should consider all the wanted signals and unwanted noises on the traces, equally. Where transmission line techniques turn out to be required for signals that do not need to have very high frequencies, or very small rise/fall times, an alternative is to low-pass filter their sources, using an RC or LC filter as discussed in [6].

More than 30 types of PCB transmission lines can easily be created for 'single-ended' power and signals, by controlling the geometry and stack-up of the traces and planes, and some of the more common types are shown in Figure 5P.

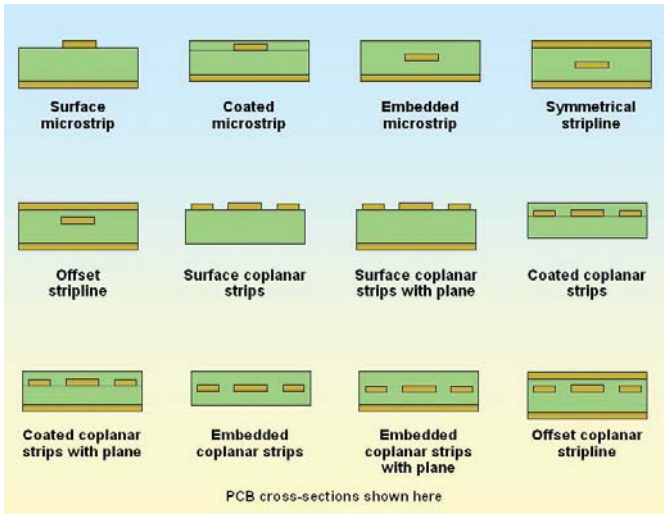

Figure 5P Some types of PCB transmission lines for single-ended signals or power

Figure 5Q focuses on the 'surface microstrip' type of transmission line, and gives the simplest equation that can be used for calculating its characteristic impedance, Z_0. Microstrips are quite complicated structures, because a fraction of the wave energy that is the propagating signal travels in the air at about twice the velocity of the remainder that travels under the trace, inside the dielectric. So the simple equation is only valid over a range of trace geometries, which nevertheless meets most normal requirements.

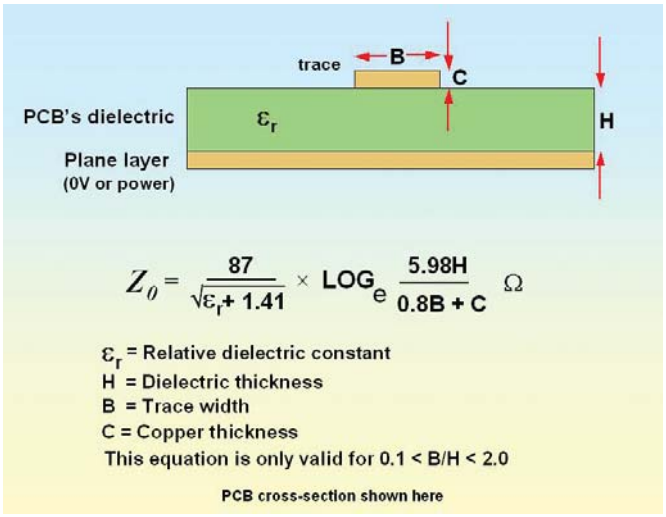

Figure 5Q Example of a 'surface microstrip'

Figure 5R focuses on the example of a 'symmetrical stripline', and gives its simplest equation for calculating Z_0. Striplines are traces that lie between two planes, and the planes do not have to be at the same potential. As described in 5.4 and 5.5, parallel 0V planes should be bonded together at least every $\lambda/10$ at f_{max} by vias, and power planes should have decaps every $\lambda/10$ at f_{max} to the main (most unbroken) 0V plane, and this is also important for striplines. λ should take the board's ε_r into account, so these spacings are equivalent to approximately $15/f_{max}$ metres for an FR4 board, when f_{max} is in MHz (e.g. 30mm for an f_{max} of 500MHz).

Striplines have better EMC characteristics than microstrip.

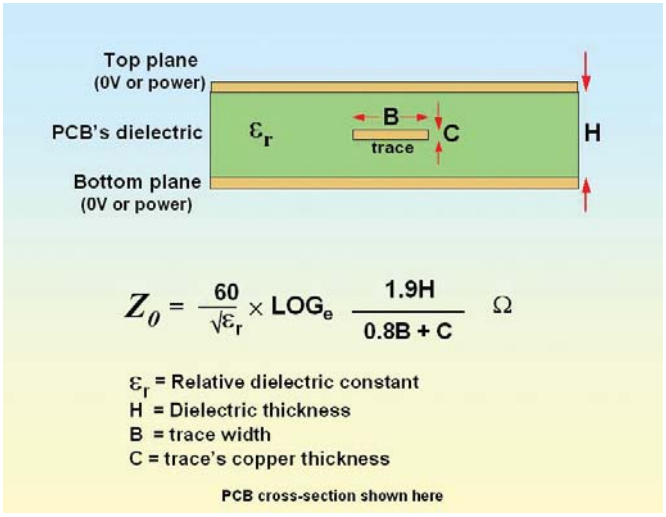

Figure 5R Example of a 'symmetrical stripline'

Because there are so many different types of transmission line that can be designed on a PCB, and because they all have different equations, it is now much more cost-effective to use a computer simulator PCB transmission-line Z_0 'solver', some of which are available free on the Internet [11]. Of course, you always get what you pay for, and the better computer simulators (e.g. those from Polar Instruments) can take into account all of

the PCB manufacturing issues that can influence the final Z_0 (e.g. areas of the PCB where the ε_r varies due to the effect of manufacturing processes on the dielectric materials in the stack-up).

Relying instead on formulae from textbooks and standards, it would be difficult to get through a dozen different stack-ups and geometries in a day (most designers seem to give up after the first six, and settle for the best of the few they have calculated).

With a fully-featured transmission line solver it is a simple matter to click on the style of transmission line to be calculated, fill in its spreadsheet with the few dimensions needed, and have the result calculated within 1 second. In this way it is possible to evaluate *many* dozens of different PCB stack-ups and trace geometries in an hour. Productivity is higher, and design quality, SI and EMC are much better.

In real PCBs, transmission lines might change their geometry along their length, and/or change layers in the stack-up. It is important to change the trace width (if required) to maintain the same value of Z_0 for each different segment of the line.

A great deal of useful information on transmission lines is given in IPC-2141 and IPC-D-317A (www.ipc.org), and also in IEC 61188-1-2 (www.iec.ch), all available to buy on-line. [12] is an excellent reference for the basics, and it includes a number of other useful references.

5.6.2 Correcting for load capacitance

The capacitances of the active devices (e.g. the input capacitances of gates, typically 3-5pF) connected to a trace cause the propagation velocity to reduce, and they also reduce the Z_0 of the trace. This is not calculated by transmission line solvers, which only take the PCB itself into account. The following formula can be used to estimate the effect of device loading:

$$Z_0\,\text{(loaded)} = \frac{Z_0}{\sqrt{(1 + C_d/C_0)}} \qquad v\,\text{(loaded)} = \frac{v_0}{\sqrt{(1 + C_d/C_0)}}$$

where: C_d is the load capacitance per unit length
C_0 is the intrinsic (bare-board) line capacitance per unit length
v_0 is the intrinsic (bare-board) line velocity

For example, if there were 6 devices, each with an input capacitance of 5pF, connected along a 200mm long trace being designed as a matched transmission line, then the value for C_d would be 150pF/metre, or 0.15pF/mm.

Except when using very thin, narrow traces, it is usually possible to reduce the width of the transmission line trace either side of the point of connection of a device, to compensate for the added capacitance at that point, so that the Z_0 of the trace can be maintained. The trace should be subdivided into sections having propagation times no longer than $t_r/10$ (for good SI) or $t_r/40$ (for good EMC) and the trace geometry adjusted to maintain the same Z_0 in each section.

IEC 61188-1-2:1998 gives formulae for C_0 and v_0, for some common types of transmission line – but it is now much better, quicker, and more accurate to extract these parameters from actual PCB layouts by using field solvers running on personal computers.

5.6.3 Choosing the dielectric materials for the stack-up

FR4 has a nominal ε_r of 4.7 at the usual measurement frequency (100kHz). But different batches can vary between 4.0 and 5.5, and some poor quality board materials can apparently vary over this range over the length or width of an individual panel. ε_r reduces as f increases, and it is nominally 4.2 at frequencies above 1MHz (but varying in practice over the range 3.6 to 4.9).

Grades of FR4 with a more accurately controlled ε_r are readily available for the construction of PCBs with matched transmission lines (known as 'controlled impedance' boards), if you know to ask for them. The author's favourite prototype board manufacturer buys a material specified as having an ε_r of 4.7 ±0.1, at 100kHz, and the extra cost is so low that they don't bother to increase the price of the prototypes.

There are many other PCB dielectrics than FR4 that may be more suitable for a particular application, for example high voltage, high temperature, high vibration, etc. There are also specialist materials designed for boards carrying microwave signals, although as the volume manufacturers of cellphones and personal computers continue to raise their data rates, techniques are being developed to use the (low cost) FR4 substrate at ever higher frequencies.

Board manufacturers purchase dielectrics in sheets, either with no copper plating, plating on one side or both, and in various thicknesses, to stack up to make a PCB. These sheet materials are only available in a limited range of thicknesses, so it is important to discuss with the chosen board manufacturer what sheet thicknesses are available, then design the trace widths and geometry accordingly.

5.6.4 Terminating transmission lines in a *matching resistance*

To function correctly as a matched transmission line, a trace that is designed as a transmission line *must* be terminated in a resistance equal to its Z_0, and for good EMC the termination resistors must maintain their overall impedance right up to f_{max}. This usually means using small SMD 'chip' resistors (not MELF types), surface-mounted resistor arrays, or integrated transmission-line termination devices, all with direct connections to the relevant planes as shown in Figure 5G.

There are a number of different transmission-line matching techniques available, all with different engineering compromises. These are described in section 2.7.3 of [7] and will not be repeated here.

5.6.5 Differential matched transmission lines

Differential signalling (also known as 'symmetrical' or 'balanced' signalling), uses two signal conductors driven in antiphase, as shown in Figure 5S. It is increasingly used on PCBs for microprocessor clocks and serial datacommunications, to improve signal integrity, and it can also – if carefully designed – provide better EMC (lower emissions, higher immunity).

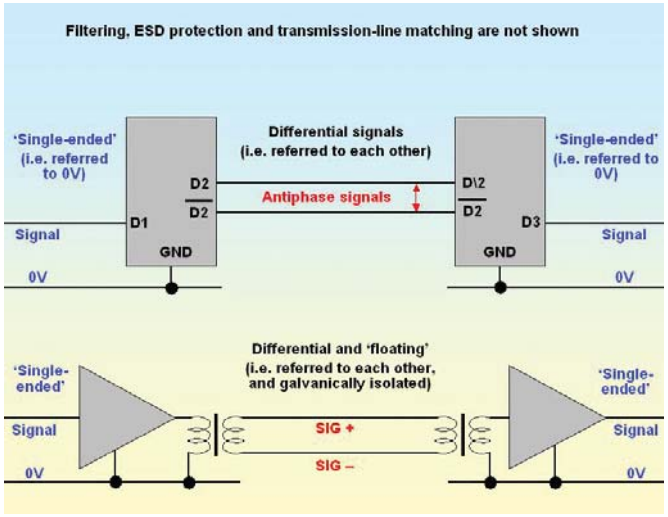

Figure 5S Examples of differential signalling

Differential signalling requires the creation of differential matched transmission lines on the PCB, which are pairs of traces routed close together along their entire route, maintaining their specified characteristic impedance values for each segment along their entire length. Differential transmission lines have *three* types of Z_0…

The single-ended Z_0, when each trace is driven independently
The CM Z_0, when both traces are driven with a common signal
The differential-mode (DM) Z_0, when the two traces are driven with antiphase signals

More than 30 types of differential PCB transmission lines can easily be created for power or signals, by controlling the geometry and stack-up of the traces and planes, as shown in Figure 5T.

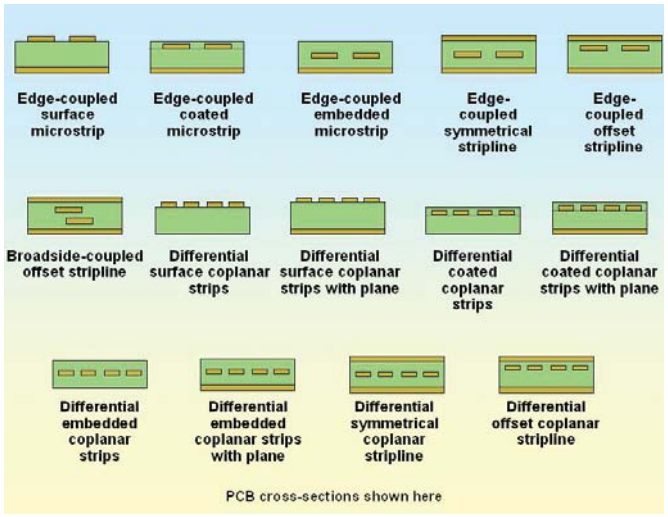

Figure 5T Some types of differential PCB transmission lines

Differential transmission lines suffer from imbalances that increase their emissions and worsen their immunity. Cables deal with similar imbalances by twisting their conductors, but of course this is almost never practical for PCB traces. Imbalances can be caused by:

- Routing too close to metalwork, edges of planes, other traces, etc., because one trace has more stray C or stray mutual inductance than the other. The use of stripline and/or coplanar techniques can help, by 'shielding' the traces above and below, and/or on both sides.

- Not maintaining the trace separation, widths, etc. so that all three types of Z_0 are maintained at the same time.

- Connectors. So choose pins that are symmetrical with respect to the shell and other pins, and so have identical stray capacitances.

It is common when terminating differential lines with matching resistors, simply to terminate the differential signals. But for good EMC all three types of Z_0 need to be correctly terminated, as shown in Figure 5U for an example of parallel (shunt) termination. Real differential signals can contain significant amounts of single trace, CM and DM signals, and unless all three modes are matched properly, emissions will be higher and immunity poorer than they need be.

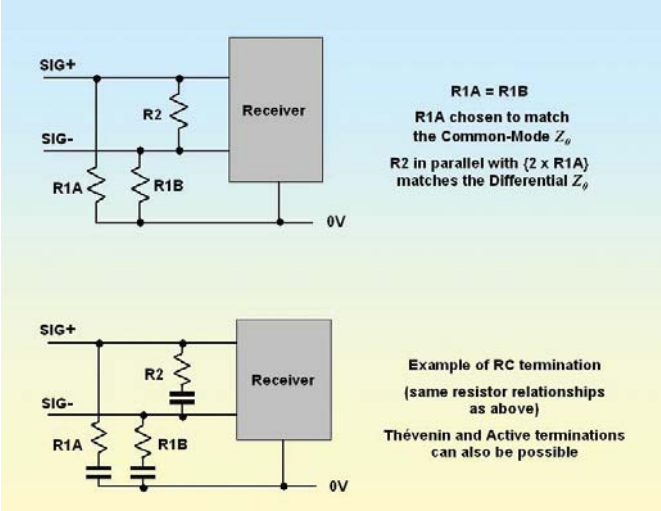

Figure 5U Examples of differential termination

5.6.6 Transmission line routing

These routing guidelines are also relevant for any traces carrying high-speed or RF signals or noises, and assume the board has at least one 0V/power plane pair in its layer stack.

- Firstly, route the 0V, power and decoupling. Because the correct use of 0V and power planes removes the need for all but the shortest traces, this will use up very little routing space and block off very little of the board area.

- Secondly, route the traces with the fastest digital edges or highest frequencies, using one PCB layer only, and keeping them short. Ideally, this would be a layer adjacent to a 0V plane that was part of a 0V/power plane adjacent pair. These traces typically include: microprocessor clocks; write strobes on SRAMs and FIFOs; output enables and chip enables and high-speed serial data buses. It can be good to route any very sensitive signal traces in a similar manner.

- Thirdly, route any parallel data busses.

- Lastly, fit all the other traces in somehow.

Design the traces and PCB layer stack to maintain the desired Z_0 over each segment of the entire length of each trace. The trace should be subdivided into sections with propagation delays

no longer than $t_r/10$ (for good SI only) or $t_r/40$ (for good EMC), and the trace geometry adjusted to maintain the same Z_0 in each section.

If a transmission line has to change layers and/or crosses a plane split, so that its adjacent plane(s) are now different, a path *must* be provided for its return current, very close indeed to the point where the trace changes planes, as described in 5.4.5.

5.6.7 Stubs and branches

Ideally, transmission lines should have no joints along their lengths, because of the impedance discontinuities these cause. This is only possible for traces that are routed point-to-point, as shown in Figure 5V. Note that when two loads are to be driven point-to-point from one driver, they should fan out from the driver pins, not from the series line matching resistors. Each load must have its own line matching resistor, and each driver output must be powerful enough to drive the parallel impedance resulting from all the lines connected to it.

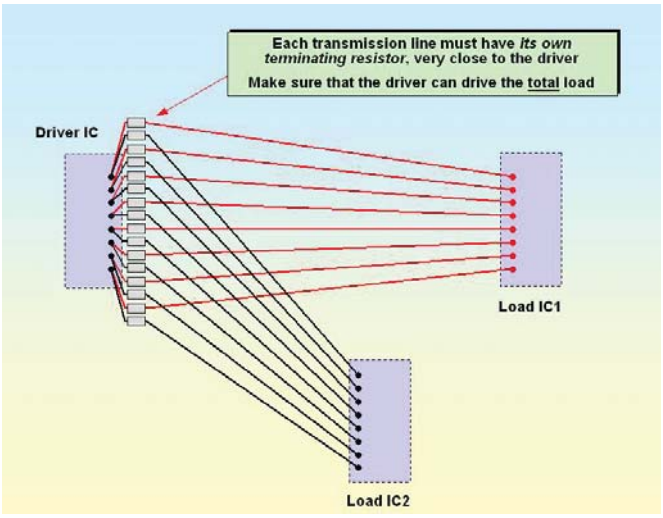

Figure 5V Example of 'star routing' using series line terminations

Decades ago, arrays of memory ICs used to be connected to data buses using a 'grid' or 'mesh' routing as shown in Figure 5W. But this is not acceptable these days because the rise-times of the ICs are so much less that serious signal degradation would occur, causing problems for SI, and much worse problems for EMC. Instead, we use 'daisy chain' routing as shown in Figure 5W, where the transmission line is routed to each IC in turn.

Of course, the vias, pins, lead frames and bond wires associated with the daisy-chained ICs act as short stubs or branches along the line, but as long as their source-to-load propagation delay is less than $t_r/20$, they can be treated as 'lumped' capacitances as described in 5.6.2. Longer stubs or branches cause serious problems for SI, and of course for EMC.

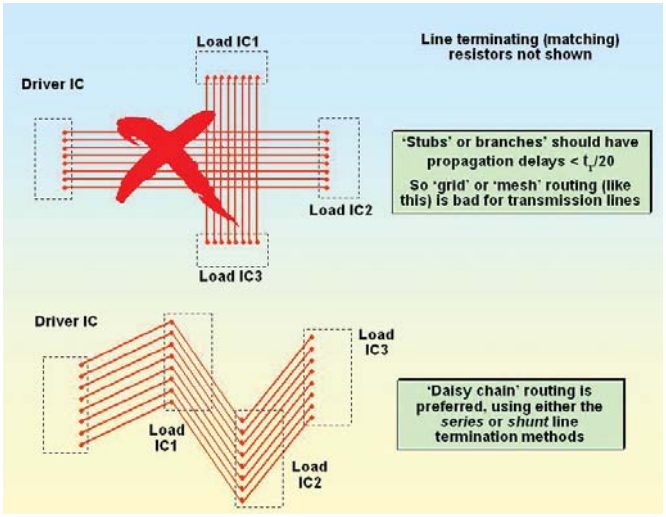

Figure 5W Example of 'daisy chain' routing

So far, this section has concerned itself with products consisting of a single PCB. But it is common for products to be made of plugged-together modules, using backplane boards, or daughterboards plugged into a motherboard. Figure 5X sketches the issues when a transmission line is used to interconnect a number of modules or daughterboards.

The lengths of the stubs or branches created by the modules or daughterboards limits the rise-time of the system and hence the maximum data rate. As mentioned above they need to have propagation times (sometimes called 'flight times') of less than $t_r/20$, and this is made more difficult for the example in Figure 5X because of the lengths of the pins in the module or daughterboard connectors. The backplane drivers and receivers are placed very close to the connectors to limit the overall stub lengths so that faster rise-times and hence faster data can be used.

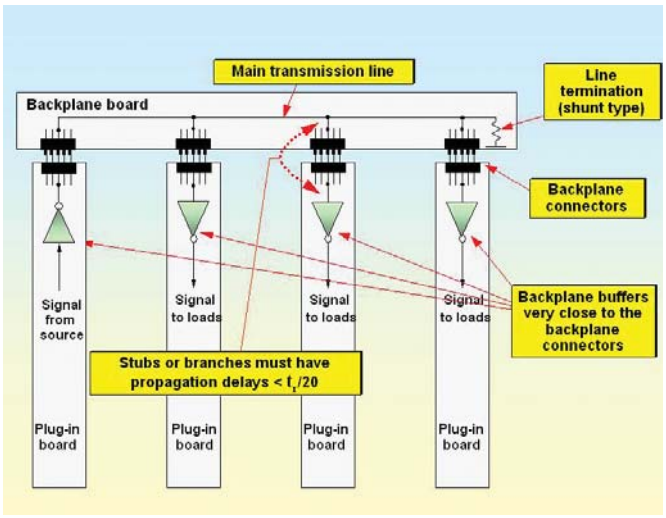

Figure 5X Example of transmission line techniques with plug-in modules

Where a stub or branch in a transmission line has a propagation delay longer than $t_r/20$, a buffer should be added at the point where it connects, so that instead of a long stub or branch it is instead a new transmission line. This technique could be applied to the example in Figure 5X, by fitting buffers on the backplane to drive the module connectors with new transmission lines.

For good EMC at board level, the "propagation delay no longer than $t_r/20$" guide above should be replaced by a "propagation delay no longer than $t_r/80$".

5.7 Layer stacking

Due to successive die shrinks over the years it is now not uncommon for fairly simple HCMOS 'glue logic' boards clocking at 40MHz (say) to fail emissions tests at over 700MHz. As described in 5.5.3, an adjacent 0V/power plane pair is required in a board's the stack-up to improve the emissions and immunity of its PDS above 300MHz – so the use of such plane pairs is assumed in this section.

With the above assumption, a 4-layer board's stack-up would be as shown in Figure 5Y.

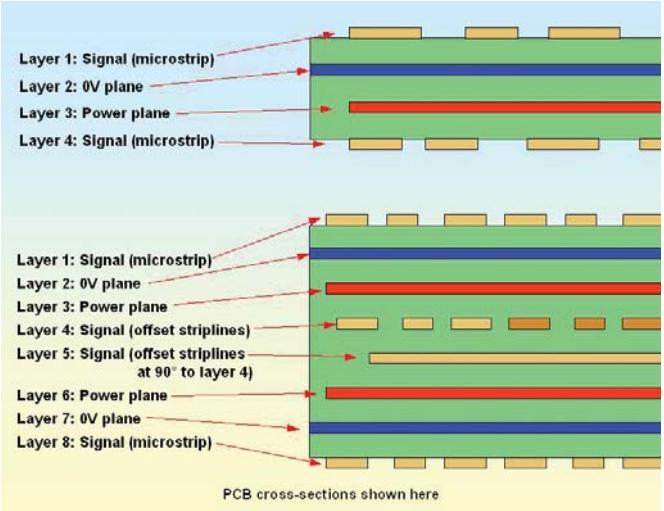

Figure 5Y Examples of 4 and 8 layer stack-ups

A 4-layer board with equally-spaced layers and a symmetrical stack-up, to help prevent board warp during automated soldering is not the best for EMC, because its 0V/power plane pair are not very close together, and not very close to the component mounting layers. Closer plane-pair spacings and closer spacings to the outer layers in the stack-up all help improve decoupling above 300MHz.

There are many possible permutations of unequal and/or unsymmetrical layer stacking in 4-layer boards. And there are also many possible permutations of layers for 6-layer boards. But only a board with 8 layers (or more) can satisfy all of the good practice EMC requirements and have a symmetrical stack-up to prevent board warp, and Figure 5Y gives an example.

Closer layer spacing is better. Spacings of 0.15mm (6 thousands of an inch) or less between traces and planes in a layer stack, and between 0V/power plane pairs, can significantly improve decoupling, reduce emissions and improve immunity (and improve SI).

So avoiding the traditional equally-spaced layer stacking can be very good for EMC, but we still want to have a symmetrical stack-up to help prevent board warp during automated soldering. Figure 5Z sketches an example of an 8-layer board with a stack-up designed in this way. Its two closely-spaced 0V/power plane pairs, close to the outer layers of the PCB, provide excellent high-frequency decoupling for components mounted on either side of the PCB.

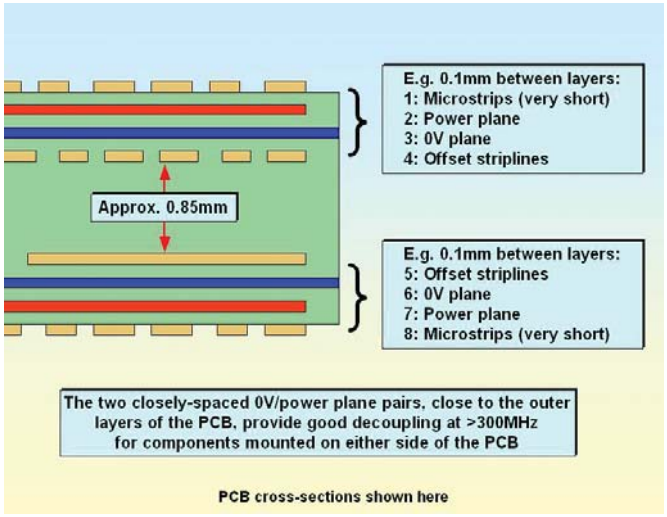

Figure 5Z Example of a close-layer-spacing but symmetrical 8 layer stack-up

The stack-up in Figure 5Z has proven to be very effective at solving difficult EMC problems at lowest cost in recent years. It is recommended for all new designs that need to mount active digital or high frequency analogue devices on both sides of the board.

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c) Microwave Office TX-Line Transmission Line Calculator: http://web.appwave.com/Products/Microwave_Office/Feature_Guide.php?bullet_id=9.
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